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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,866	07/30/2003	Jae-Jun Lee	SEC.1058	7366

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EXAMINER	
KIM, DANIEL Y	
ART UNIT	**PAPER NUMBER**
2185	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,866	LEE ET AL.	
	Examiner	Art Unit	
	Daniel Kim	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *July 30, 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. 2002-0045914.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Objections - Specification

1. On page 5, line 6, the word "precense" is spelled incorrectly. It appears that "precense" should be changed to "presence". Appropriate correction is required.

Objections - Claims

2. In claim 1, lines 8-9, "the SIMM" and "the DIMM" fail to account for the possibility of a plurality of SIMMs or DIMMs, as suggested previously in the claim. It is suggested that the phrases "the SIMM" and "the DIMM" are changed to "the at least one SIMM" and "the at least one DIMM", respectively.

In claim 2, lines 2 and 5, "memory devices of the SIMM" fail to account for the possibility of a singularity of SIMMs, as suggested in claim 1, on which claim 2 depends. It is suggested that this phrase is changed to "the at least one memory device of the at least one SIMM".

In claim 3, lines 2-3 and 5-6, "the SIMM" and "the DIMM" should be changed similar to claim 1 above. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6, 7, 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 6, lines 4-6, the applicant fails to describe what the longer length of the first signal transmission line of the first memory module compensates for in the fourth signal transmission line connected between first and second sockets. It is not possible to evaluate this portion of the claim based on prior art because the above language is awkward and ambiguous. For purpose of examination, this portion of the claim has not been considered on the merits.

Claims 7, 10 and 11 are rejected by virtue of their dependencies on claim 6.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abe (US PGPub No. 20030049949), Leddige et al (US Patent No. 6144576) and Dixon et al (US Patent No. 6081862).

For claim 1, Abe discloses a memory system comprising:

at least one single in-line memory module (SIMM) including at least one memory device and a signal transmission line connected between the memory device and a connection terminal (a plurality of memory slots each of which has a structure for accepting a memory module... and includes a plurality of connector terminals for being in contact with module pins formed in said memory module; a memory bus which includes a plurality of signal lines coupled to at least one connector terminal of each of said plurality of memory slots, par. 0019-0020, note that memory modules may be SIMM or DIMM, par. 0077 and 0117); and

at least one dual in-line memory module (DIMM) including at least two memory devices and a signal transmission line connected between the two memory devices and a connection terminal (par. 0019-0020, in addition to par. 0077 and 0117).

For claim 1, Abe does not expressly disclose a longer length of SIMM signal transmission line than that of a DIMM.

Leddige et al (hereafter referred to as Leddige) discloses that the length of a signal line determines the electrical delay and capacitance (and equivalently, load) on the signal line. It is to be noted that for one of ordinary skill in the art, it is common knowledge that differences in electrical delay and capacitance between signal lines may adversely affect the performance of devices connected to the signal lines that operate at high speeds, that SIMM configurations require relatively long wires, and that with DIMMS, long transmission lines may present timing problems.

Abe and Leddige are analogous art in that they are in the same field of endeavor, that is, memory systems for high speed, stable transmission of signals between

devices. It would have been obvious to a person of ordinary skill in the art at the time of the invention to allow a SIMM to have a longer length of transmission line than the DIMM, since this is one method of compensating for timing problems as a result of differing delay times and loads between these memory devices (col. 1 lines 66-7 col. 2 lines 1-4), as taught by Dixon.

6. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe, Leddige and Dixon as applied to claim 1 above and further view of Doblar et al (US PGPub No. 20030043613).

For claim 2, Abe discloses the memory system of claim 1, but does not expressly disclose that the load of memory devices of the SIMM is less than the load of the memory devices of the DIMM. Doblar et al (hereafter referred to as Doblar), however, discloses that the total load on a signal driver includes the sum of the chip inputs connected to the line (par. 0006), and that SIMMs have opposing contact pads are connected together (i.e. shorted), and thus carry the same signal, while at least some of the opposing contact pads on DIMMs are not connected, thus allowing different signals to be carried (par. 0005).

Abe and Doblar are analogous art in that they are in the same field of endeavor, that is, improvement upon signal transmission in memory systems. It would have been obvious to a person of ordinary skill in the art at the time of the invention that the load of memory devices of a SIMM are less than the load of memory devices on a DIMM because a DIMM has a greater sum of contact pads, or equivalently, chip inputs, which result in a greater load (par. 0005-0006), as taught by Doblar.

Claim 4 is rejected using the same rationale as for the rejection of claim 1 above. Abe further discloses:

a memory controller (par. 0079);

a first memory module including at least one first memory device and a first signal transmission line connected between the at least one first memory device and a connection terminal (a plurality of memory slots each of which has a structure for accepting a memory module... and includes a plurality of connector terminals for being in contact with module pins formed in said memory module; a memory bus which includes a plurality of signal lines coupled to at least one connector terminal of each of said plurality of memory slots, par. 0017-0018, note that memory modules may be SIMM or DIMM, par. 0077 and 0117);

a second memory module including at least one second memory device and a second signal transmission line connected between the at least one second memory device and a connection terminal (par. 0017-0018 again), and

first and second sockets which are connected to the memory controller and which respectively receive the connection terminals of the first and second memory modules (a memory controller which is coupled to a plurality of memory chips on a memory module inserted in at least one of said plurality of memory slots, through a memory bus, par. 0021).

7. Claims 3 and 5-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abe (US PGPub No. 20030049949), Leddige, Dixon and Doblar as applied to claim 2 above and further view of Ono et al (US PGPub 20020041020).

For claim 3, Abe further discloses a first socket which receives the connection terminal of the SIMM (a plurality of memory slots each of which has a structure for accepting a memory module... and includes a plurality of connector terminals for being in contact with module pins formed in said memory module, par. 0019); note that memory modules may be SIMM or DIMM, (par. 0077 and 0117); a second socket which receives the connection terminal of the DIMM (par. 0019, 0077 and 0117 again); and a signal transmission line connected between the first and second sockets (a memory bus which includes a plurality of signal lines coupled to at least one connector terminal of each of said plurality of memory slots, par. 0020).

For claim 3, Abe does not expressly disclose the longer length of the signal transmission line of the SIMM increases the signal delay time of the SIMM to further compensate for the signal transmission line connected between the first and second sockets.

Ono, however, discloses that in a bus having multiple slots, the degree of influence to the waveforms that the reflected waves give at the termination greatly differs at the socket near side or at the socket far side, which makes the timing design difficult. And, as the number of the sockets increases, the length of the bus wiring becomes longer, and the wiring capacity (and equivalently, load) increases, which makes it unfit for a high speed operation. Therefore, a shorter bus wiring with a shorter distance between the sockets in addition will achieve a better characteristic (par. 0009).

Abe, Leddige, Dixon and Ono are analogous art in that they are in the same field of endeavor, that is, improvement upon signal transmission in memory systems. It

would have been obvious to a person of ordinary skill in the art at the time of the invention that a longer length of the signal transmission line of a SIMM increases the signal delay time of the SIMM to compensate for the transmission line connected between sockets because wiring between sockets increases load, and lengthening the signal transmission line of the SIMM is one method of compensating for these timing problems as a result of differing delay times and loads (col. 1 lines 66-67 and col. 2 lines 1-4), as taught by Dixon.

Claim 5 is rejected using the same rationale as for the rejection of claims 3 and 4 above.

Claim 6 is rejected using the same rationale as for the rejection of claim 3.

As for a signal transmission line connected between the memory controller and a first socket, Abe discloses a memory controller that is coupled to a plurality of memory chips on a memory module inserted in at least one of a plurality of memory slots, through a memory bus (par. 0032).

As for a signal transmission line connected between the first socket and the second socket, Abe discloses a memory bus which includes a plurality of signal lines coupled to at least one of a plurality of connector terminals of each of a plurality of memory slots (par. 0031).

Claim 7 is rejected using the same rationale as for the rejection of claim 3.

As for an impedance matching resistive element, Abe discloses an example of an impedance matching circuit (par. 0092, fig. 2 items 2A, 3A, 4A, 7A).

Claim 8 is rejected using the same rationale as for the rejection of claim 4.

Claim 9 is rejected using the same rationale as for the rejection of claim 4.

Claim 10 is rejected using the same rationale as for the rejection of claim 3.

Claim 11 is rejected using the same rationale as for the rejection of claim 3.

Contact Information

8. Any inquiries concerning this action or earlier actions from the examiner should be directed to Daniel Kim, reachable at 571-272-2742, on Mon-Fri from 8:30am-5pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan, is also reachable at 571-272-4210. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information from published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. All questions regarding access to the Private PAIR system should be directed to the Electronic Business Center (EBC), reachable at 866-217-9197.

DK

10-14-05

PIERRE VITAL
PRIMARY EXAMINER